Electronic Version
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Claims

[c1] What is claimed is:

1.A flash memory cell structure comprising:

a substrate having a stacked gate;

a select gate formed on the substrate and adjacent to one side of the stacked gate;

a first-type doped region located in the substrate and adjacent to the select gate as a drain;

a shallow second-type doped region located underneath the stacked gate and adjacent to the first-type doped region;

a deep second-type doped region surrounding the first-type doped region and adjacent to the shallow second-type doped region; and

a doped source region formed on a side of the shallow second-type doped region as a source.

[c2] 2.The flash memory cell structure of claim 1 wherein a depth of the deep second-type doped region is deeper than a depth of the shallow second-type doped region.

[c3] 3.The flash memory cell structure of claim 1 wherein the deep second-type doped region has the same doped ions as the shallow second-type doped region.

[c4] 4.The flash memory cell structure of claim 3 wherein the doped ions of the deep second-type doped region and the shallow second-type doped region are selected from the III A group.

[c5] 5.The flash memory cell structure of claim 1 wherein the doped ions of the first-type doped region and the doped source region are selected from the V A group.

[c6] 6.The flash memory cell structure of claim 1 wherein the first-type doped region and the deep second-type doped region are electrically short-circuited together.

[c7] 7.The flash memory cell structure of claim 6 wherein the first-type doped region and the deep second-type doped region are electrically short-circuited by metal penetrating the junction between the first-type doped region and the deep second-type doped region.

[c8] 8.The flash memory cell structure of claim 6 wherein the first-type doped region and the deep second-type doped region are electrically short-circuited by metal exposed outside the first-type doped region and the deep second-type doped region of the substrate.

[c9] 9.The flash memory cell structure of claim 1 wherein the stacked gate includes a floating gate located over the

shallow second-type doped region, and a control gate located over the floating gate.

[c10] 10.A method of operating a flash memory cell structure, the flash memory cell structure comprising a substrate, a select gate, a first-type doped region, a shallow second-type doped region, a deep second-type doped region, and a doped source region, the substrate having a stacked gate including a control gate, the select gate being formed on the substrate and adjacent to a side of the stacked gate, the first-type doped region being located in the substrate and adjacent to the select gate as a drain, the shallow second-type doped region surrounding the first-type doped region and being short-circuited to the shallow second-type doped region, the doped source being located on a side of the shallow second-type doped region as a source, the method comprising:
applying a high voltage to the control gate, applying a voltage relatively lower than the voltage applied to the control gate to the drain, floating the source, and grounding the select gate in a programming process;
applying a low voltage to the control gate, applying a voltage relatively higher than the voltage applied to the control gate to the select gate, and floating the source and the drain in an erasing process; and
applying a word line voltage to the control gate, applying

a voltage relatively lower than the word line voltage to the source, grounding the drain, and applying a power voltage to the select gate in a reading process.

[c11] 11.The method of claim 10 wherein the flash memory cell structure is a NOR type flash memory cell structure.

[c12] 12.A method of operating a flash memory cell structure, the flash memory cell structure comprising a substrate, a select gate, a first-type doped region, a shallow second-type doped region, a deep second-type doped region, and a doped source region, the substrate having a stacked gate including a control gate, the select gate being formed on the substrate and adjacent to a side of the stacked gate, the first-type doped region being located in the substrate and adjacent to the select gate as a drain, the shallow second-type doped region surrounding the first-type doped region and being short-circuited to the shallow second-type doped region, the doped source being located on a side of the shallow second-type doped region as a source, the method comprising: applying a high voltage to the control gate, applying a voltage relatively lower than the voltage applied to the control gate to the source, applying a voltage relatively lower than the voltage applied to the source to the select gate, and grounding the drain in a programming process;

applying a low voltage to the control gate, applying a voltage relatively higher than the voltage applied to the control gate to the drain, floating the source, and grounding the select gate in an erasing process; and applying a word line voltage to the control gate, applying a voltage relatively lower than the word line voltage to the source, applying a power voltage to the select gate, and grounding the drain in a reading process.

[c13] 13.The method of claim 12 wherein the operations of the flash memory cell structure are performed in a manner of byte program and byte erase.

[c14] 14.A method of operating a flash memory cell structure, the flash memory cell structure comprising a substrate, a select gate, a first-type doped region, a shallow second-type doped region, a deep second-type doped region, and a doped source region, the substrate having a stacked gate including a control gate, the select gate being formed on the substrate and adjacent to a side of the stacked gate, the first-type doped region being located in the substrate and adjacent to the select gate as a drain, the shallow second-type doped region surrounding the first-type doped region and being short-circuited to the shallow second-type doped region, the doped source being located on a side of the shallow second-type doped region as a source, the method comprising:

applying a low voltage to the control gate, applying a voltage relatively higher than the voltage applied to the control gate to the drain, floating the source, and grounding the select gate in a programming process; applying a high voltage to the control gate, applying a voltage relatively lower than the voltage applied to the control gate to the source, floating the drain, and grounding the select gate in an erasing process; and applying a word line voltage to the control gate, applying a voltage relatively lower than the word line voltage to the source, applying a power voltage to the select gate, and grounding the drain in a reading process.

[c15] 15.The method of claim 14 wherein the flash memory cell structure is a BiNOR type flash memory cell structure.

[c16] 16.The method of claim 14 wherein the word line voltage is identical to the power voltage in the reading process.